Remarks:

Reconsideration of the application is requested.

Claims 1-12 and 14-17 remain in the application. Claims 1, 2, 4, 5, and 17 have been amended. Claim 18 has been cancelled. Claims 5-6, 8, and 14-16 have withdrawn from consideration.

We note that there is a US patent, *Dagostino et al.* (US 5,418,470) corresponding to the reference EP 0650 069 A2 cited in the filed IDS. We therefore enclose a copy of *Dagostino et al.* with the response, for placement in the file wrapper.

In item 1 on page 2 of the above-identified Office action, the Examiner stated that appropriate action is required in regard to the non-elected claims 5-6, 8, and 14-16.

Withdrawn claims 5-6 and 8 depend on elected claims, and therefore these claims ultimately dependent on claim 1. Should claim 1 be held allowable, the Examiner must withdraw the election requirement in regard to claims 5-6 and 8. Therefore, the claims have not and should not be cancelled.

In item 5 on page 3 of the Office action, claims 1-4, 7, 9-12, and 17-18 have been rejected as being anticipated by *Palagonia* (US 5,895,978) under 35 U.S.C. § 102.

The rejection and the Examiner's comments have been considered. Consequently, the claims have been amended in an effort to even more clearly define the invention of the instant application.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 1 (similarly claim 17) as amended calls for, inter alia:

> An integrated circuit component, comprising:
>
> a plurality of circuit points not being directly externally accessible, ***providing a reference signal provided by the integrated circuit component*** for test purposes, and various electrical signals of the integrated circuit component to be monitored for test purposes;
>
> at least one connecting contact point being externally accessible; and
>
> a multiplexer having an output connected to said at least one connecting contact point and having a plurality of inputs, each one of said plurality of inputs being connected to a respective one of said plurality of circuit points, thereby granting external access to the reference signal and to the various electrical signals.

In the *Response to Arguments* on page 2 of the Office action, the Examiner stated that:

> Applicant's arguments filed 08/29/2003 have been fully considered but they are not persuasive. At page 18 applicants argues that "*Palagonia* does not show at least one connecting contact point externally accessible for monitoring electrical signals ***for test purpose*** as recited in claims I and 17 of the instant application". Examiner disagrees because, 1) claim 1 is amended to include above limitation, Palagonia at lines 56-62 on column 3 and 11-16 of column 4 suggests the testing of die 40, and 2) claim 17 does not recite those limitation and hence it is not valid argument for claim 17. Applicant have amended claim 18 (which depend from claim 17) to include above limitation. Palagonia at lines 56-62 on column 3 and 11-16 of column 4 suggests the testing of the die 40 ***where terminals 42A is externally available to interposer 10***.

(Emphasis original.)

Col. 3, lines 56-62, of *Palagonia* states:

> This clock and the accompanying MUX control signals can be generated in three places, externally, on the interposer, or on the die, in which case the clock could be a standard die clock or a special die/interposer clock. An implementation of the clock and die/interposer MUX control on the interposer is preferred for reasons of testability, ease of fabrication and inventory cost.

Col. 4, lines 11-16, of *Palagonia* states:

> Each interposer MUX 22 in turn is wired to a interconnect pad 26A by a land 34. ***Interposer pads 20B provide external clock and control signal access*** to interposer clock and control logic 24 by lands 36. Lands 35 carry clock and control signals from interposer clock and control logic 24 to interconnect pads 26B. Multi wire bus 38 carries clock and control signals to interposer MUX's 22.

(Emphasis added.)

Hence, the Interposer pads 20B in *Palagonia* serve only for ***inputting*** external clock and control signal access, but not for ***outputting*** a reference signal produced within and by the integrated circuit component for test purposes.

Clearly, *Palagonia* does not show a reference signal as recited in claims 1 and 17 of the instant application. Therefore, the invention as recited in claims 1 and 17 of the instant application is believed not to be anticipated by *Palagonia*.

It is accordingly believed to be clear that *Palagonia* do not show the features of claims 1 and 17. Claims 1 and 17 are, therefore, believed to be patentable over the art and because 2-12 are ultimately dependent on claim 1, they are believed to be patentable as well.

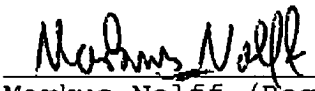
In the event the Examiner should still find any of the claims to be unpatentable, the Examiner is respectfully requested to telephone Counsel so that, if possible, patentable language can be worked out. In the alternative, the entry of the amendment is requested as it is believed to place the application in better condition for appeal, without requiring extension of the field of search.

In view of the foregoing, reconsideration and allowance of claims 1-12 and 17 are solicited.

If an extension of time is required, petition for extension is herewith made.

Please charge any fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,



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US005418470A

United States Patent [19]

Dagostino et al.

[11] Patent Number: 5,418,470

[45] Date of Patent: May 23, 1995

[54] ANALOG MULTI-CHANNEL PROBE SYSTEM

[75] Inventors: Thomas P. Dagostino, Beaverton; Arnold M. Frisch, Portland; both of Oreg.

[73] Assignee: Tektronix, Inc., Wilsonville, Oreg.

[21] Appl. No.: 139,681

[22] Filed: Oct. 22, 1993

[51] Int. Cl.[6] G01R 31/28

[52] U.S. Cl. 324/763; 324/158.1; 371/22.5

[58] Field of Search ..... 324/158 F, 158 R, 73.1, 324/763, 158.1; 371/22.3, 22.5, 22.6

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Primary Examiner—Ernest F. Karlsen
Attorney, Agent, or Firm—Francis I. Gray; John Smith-Hill

[57] ABSTRACT

A programmable analog multi-channel probe system is embedded within a device under test for coupling test points to external measurement points of the device under test. Programmable input buffer amplifiers are coupled to the test points to couple the data at those points to their outputs when enabled. The data from the input buffer amplifiers are input to respective routers to provide a plurality of outputs. Each common output from the routers is coupled as an input to an output buffer amplifier that provides the data as an output when enabled. The data at the output of the output buffer amplifiers is converted to a differential signal for transmission to the external measurement point by differential input/output amplifiers that have a reference level, selected from a plurality of reference levels including an internal reference level, as an input for comparison with the data from the output buffer amplifiers. A termination circuit may be provided for each output to provide appropriate impedance interface with the measurement points.

14 Claims, 2 Drawing Sheets